What is claimed is:

1. A three-level inverter apparatus comprising:

a first voltage node coupled to a neutral DC voltage source via a first diode oriented to prevent under-voltage of said first voltage node;

a second voltage node coupled to the neutral DC voltage source via a second diode oriented to prevent over-voltage of said second voltage node;

an AC output node;

a first bipolar transistor, having a first collector coupled to said first voltage node and a first emitter coupled to said AC output node, wherein said first emitter and said first collector is bridged by a third diode in a direction that allows said third diode to conduct reverse currents;

a second bipolar transistor, having a second collector coupled to said AC output node and a second emitter coupled to said second voltage node, wherein said second emitter and said second collector is bridged by a fourth diode in a direction that allows said fourth diode to conduct reverse currents;

a first field effect transistor, having a first drain coupled to a positive DC voltage source and a first source coupled to said first voltage node; and

a second field effect transistor, having a second drain coupled to said second voltage node and a first source coupled to a negative DC voltage source.

2. An inverter as in claim 1, wherein said first and second bipolar transistors are insulated gate bipolar transistors and wherein said first and second field effect transistors are metal oxide field effect transistors.

3. An inverter as in claim 2, whereby the inverter is part of an uninterruptible power supply.

4. An inverter as in claim 1 wherein said AC output node is an output of a filter stage, the output of said filter stage being for use with a load.

5. An inverter as in claim 1, wherein the inverter further comprises a control means for turning on and off said first and said second field effect transistor and said first and said

second bipolar transistor and wherein said control means supplies control signals to said transistors that differ for each of four output phase quadrants.

6. An inverter as in claim 5, wherein said control means is operative to:

modulate said first field effect transistor when said inverter is operated in a first output phase quadrant characterized by both output voltage and current being positive;

modulate said first and second bipolar transistors while said first field effect transistor is in an off state and while said second field effect transistor is in an on state when said inverter is operated in a second output phase quadrant characterized by negative output voltage and positive output current;

modulate said second field effect transistor when said inverter is operated in a third output phase quadrant characterized by both output voltage and current being negative; and

modulate said first and second bipolar transistors while said first field effect transistor is in an on state and while said second field effect transistor is in an off state when said inverter is operated in a fourth output phase quadrant characterized by negative output voltage and positive output current.

7. An inverter as in claim 6, wherein said control means is further operative to:

modulate said second bipolar transistor when said inverter is in said first output phase quadrant;

modulate said first bipolar transistor when said inverter is in said third output phase quadrant.

8. An inverter as in claim 6 wherein the control means is operative to determine the phase quadrant by determining the voltage and current through a filter choke.

9. An inverter as in claim 8 wherein the control means is operative to determine the phase quadrant to be:

said fourth quadrant when the current through said filter choke rapidly changes polarity and the voltage of said AC output node is positive;

said second quadrant when the current through said filter choke rapidly changes polarity and the voltage of said AC output node is negative.

10. An inverter as in claim 1, wherein the inverter is part of an uninterruptible power supply.

11. An inverter as in claim 1, wherein the inverter output corresponds to one output of a three-phase voltage source.

12. An inverter as in claim 1, wherein said first bipolar transistor and said third diode are in a first sealed package; and wherein said second bipolar transistor and said fourth diode are in a second sealed package.

13. A three-level inverter comprising:

an electrical output means;

a means for coupling to a positive voltage source;

a means for coupling to a negative voltage source;

a means for coupling to a neutral voltage source;

a first controlled switching means for allowing or restricting electrical current between a positive voltage source and a second controlled switching means according to a first control means;

said second controlled switching means for allowing or restricting electrical current between:

said first controlled switching means and said electrical output means according to a second control means; and

a neutral voltage source and said electrical output means according to said second control means;

a third controlled switching means for allowing or restricting electrical current between:

a fourth controlled switching means and said electrical output means according to a third control means; and

said neutral voltage source and said electrical output means according to said third control means;

said fourth controlled switching means for allowing or restricting electrical current between a negative voltage source and said third controlled switching means according to a fourth control means;

wherein said first control means is operative to actively turn said first switching means on and off when said electrical output means is operated in a first phase quadrant, said first control means further leaving said first switching means in a static state when said electrical output means is operated in each of the remaining phase quadrants;

wherein said second control means is operative to actively turn said second switching means on and off when said electrical output means is operated in a second phase quadrant and a fourth phase quadrant,

wherein said third control means is operative to actively turn said third switching means on and off complementary to said second switching means when said electrical output means is operated in said second phase quadrant and said fourth phase quadrant,

wherein said fourth control means is operative to actively turn said fourth switching means on and off when said electrical output means is operated in a third phase quadrant, said fourth control means further leaving said fourth switching means in a static state when said electrical output means is operated in each of the remaining phase quadrants.

14. A three-level inverter as in claim 13 whereby said electrical output means includes a filter means.

15. A three-level inverter as in claim 14 whereby said inverter is part of an uninterruptible power supply.

16. A three-level inverter as in claim 14 whereby said electrical output means is used to supply one of the output voltages of a three-phase system.

17. A three-level inverter as in claim 13 whereby said phase quadrants are determined by monitoring voltage and current in said electrical output means.

18. A three-level inverter as in claim 13 whereby:

said second control means is further operative to leave said second switching means in a static state when said electrical output means is operated in said first and said third phase quadrants;

said third control means is further operative to leave said third switching means in a static state complementary to said second switching means when said electrical output means is operated in said first and said third phase quadrants.

19. A three-level inverter as in claim 13 whereby:

said second control means is further operative to leave said second switching means in a static state when said electrical output means is operated in said first phase quadrant and to actively turn said second switching means on and off when said electrical output means is operated in said third phase quadrant;

said third control means is further operative to leave said third switching means in a static state when said electrical output means is operated in said third phase quadrant and to actively turn said third switching means on and off when said electrical output means is operated in said first phase quadrant.

20. A method of providing alternating current from an inverter comprising providing:

a first voltage node coupled to a neutral DC voltage source via a first diode oriented to prevent under-voltage of said first voltage node;

a second voltage node coupled to the neutral DC voltage source via a second diode oriented to prevent over-voltage of said second voltage node;

an AC output node;

a first bipolar transistor, having a first collector coupled to said first voltage node and a first emitter coupled to said AC output node, wherein said first emitter and said first collector is bridged by a third diode in a direction that allows said third diode to conduct reverse currents;

a second bipolar transistor, having a second collector coupled to said AC output node and a second emitter coupled to said second voltage node, wherein said second emitter and said second collector is bridged by a fourth diode in a direction that allows said fourth diode to conduct reverse currents;

a first field effect transistor, having a first drain coupled to a positive DC voltage source and a first source coupled to said first voltage node;

a second field effect transistor, having a second drain coupled to said second voltage node and a first source coupled to a negative DC voltage source; and

a control means for turning on and off said first and second field effect transistors and said first and second bipolar transistors; and supplying control signals to said transistors that differ for each of four output phase quadrants.

21. The method of claim 20 wherein supplying control signals comprises:

modulating said first field effect transistor while said first bipolar transistor is in an on state and while said second field effect transistor is in an off state when said inverter is operated in a first output phase quadrant characterized by both output voltage and current being positive;

modulating said first and second bipolar transistors while said first field effect transistor is in an off state and while said second field effect transistor is in an on state when said inverter is operated in a second output phase quadrant characterized by negative output voltage and positive output current;

modulating said second field effect transistor while said second bipolar transistor is in an on state and while said first bipolar transistor and said first FET are in an off state when said inverter is operated in a third output phase quadrant characterized by both output voltage and current being negative; and

modulating said first and second bipolar transistors while said first field effect transistor is in an on state and while said second field effect transistor is in an off state when said inverter is operated in a fourth output phase quadrant characterized by negative output voltage and positive output current.

22. An inverter as in claim 21, wherein said first bipolar transistor and said third diode are in a first sealed package; and wherein said second bipolar transistor and said fourth diode are in a second sealed package.

23. The method as in claim 21 further comprising monitoring the output of the inverter to determine the phase quadrant the inverter is operating in.

24. The method as in claim 23 whereby the phase quadrant is not updated until the output is determined to remain in a phase quadrant for more than one modulation cycle.

25. The method as in claim 21 wherein modulation of the first and second bipolar transistors is performed such that the first and second bipolar transistors are not both closed simultaneously during operation in any phase quadrant.

26. The method as in claim 21 wherein modulation of the first and second bipolar transistors is performed such that the first and second bipolar transistors are not both closed simultaneously during operation in the second and fourth phase quadrants.

27. The method as in claim 21 wherein modulation of the first and second bipolar transistors is performed such that the second bipolar transistor is modulated during operation in the first phase quadrant and the first bipolar transistor is modulated during operation in the third phase quadrant.